REMARKS

Favorable reconsideration of the present application is respectfully requested. Since the amendments made herein raise no new issues, and in any event, place the application in better condition for consideration on appeal, entry thereof is respectfully requested.

Before addressing the issues raised in the outstanding Office Action, Applicants have amended Claim 16 to positively recite that the fluorine doped low K dielectric oxide is in direct contact with an overlying silicon nitride oxide layer. This is supported by the specification and figures of the instant application. See, for example, FIG. 7. Also, Claim 16 has been amended to positively recite that at least a portion of source and drain regions directly contacts the silicon nitride oxide layer. This is supported by the specification and particularly by paragraph [0022] and FIG. 7 of the instant application.

Claim 20 has been amended to positively recite that the silicon nitride oxide layer covers the entirety of the top surface of the semiconductor substrate. This is supported by FIGS. 3 – 7 and accompanying passages of the instant application. Claim 21 has been amended to positively recite that the silicon nitride oxide layer of the present invention directly overlays and contacts the gate stack, the fluorine doped low K dielectric oxide gate spacer, and remaining surfaces of the silicon substrate and that no material with a dielectric constant equal to or greater than 4.0 is present the fluorine doped low K dielectric oxide gate spacer and the silicon nitride oxide layer. This is supported by FIGS. 3 – 7 and accompanying passages of the instant application. Since the amendments do not introduce new matter, entry thereof is respectfully requested.

In the outstanding Office Action, Claim 16 stands rejected under 35 U.S.C. § 102(b) as allegedly anticipated by U.S. Patent No. 5,599,726 to Pan ("Pan"). Claims 17 – 18 stand rejected under 35 U.S.C. §103 (a) as allegedly unpatentable over Pan. Claims 16 – 18 stand rejected

under 35 U.S.C. §103 (a) as allegedly unpatentable over U.S. Patent No. 6,555,829 to Horstman et al. ("Horstman") in view of Pan. Claim 20 stands rejected under 35 U.S.C. §103 (a) for allegedly unpatentable over Horstman in view of Pan and further in view of U.S. Patent 5,973,371 to Kasai ("Kasai"). Claim 21 stands rejected under 35 U.S.C. §103 (a) as allegedly unpatentable over Kasai in view of U.S. Patent Application No. 2003/0038305 to Wasshuber ("Wasshuber"). Claim 21 stands rejected under 35 U.S.C. §103 (a) as allegedly unpatentable over Wasshuber in view of Kasai.

Concerning the 35 U.S.C. § 102(b) anticipation rejection on Claim 16, it is axiomatic that anticipation under § 102 requires that the prior art reference disclose each and every element of the claim to which it is applied. In re King, 801 F.2d, 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1986). Thus, there must be no difference between the subject matter of the claim and the disclosure of the prior art reference. Stated another way, the reference must contain within its four corners adequate direction to practice the invention as claimed. The corollary of the rule is equally applicable: Absence from the applied reference of any claimed element negates anticipation. Kloster Speedsteel AB v. Crucible Inc., 793 F.2d 1565, 1571, 230 USPQ 81, 84 (Fed. Cir. 1986).

Applicants respectfully submit that Pan does not disclose the claimed structure that is recited in currently amended Claim 16. Specifically, Pan does not disclose a MOSFET device comprising a fluorine doped low K dielectric oxide gate spacer located on sidewalls of said gate stack, said fluorine doped low K dielectric oxide gate spacer having a fluorine content of about 1E14 to 2E16 cm^{-2}, wherein ***said fluorine doped low K dielectric oxide gate spacer is in indirect contact with an overlying silicon nitride oxide layer.*** According to the present invention, spacers are not conductive since it is a "dielectric oxide". According to Pan, the fluorine doped

low K dielectric oxide 18 directly contacts an overlying conducting layer 22a and 22b as shown in FIGS. 3 and 4 of Pan and as described in Column 6, line 52 through Column 7, line 44.

Furthermore, Pan does not disclose a MOSFET device comprising a fluorine doped low K dielectric oxide gate spacer located on sidewalls of said gate stack, said fluorine doped low K dielectric oxide gate spacer having a fluorine content of about 1E14 to 2E16 cm^{-2}, wherein ***at least a portion of said source and drain regions directly contacts a silicon nitride oxide layer.*** According to the present invention, "an ISSG (in-situ steam generation) oxidation process is used to convert the thin SiN etch stop to oxide, to be consistent with a low-K spacer objective" (paragraph [0031] of the instant application). "The fabrication process results in a silicon nitride oxide layer being formed over the MOSFET device" (paragraph [0043] of the instant application). As can be seen in FIG. 7 of the instant application, the fluorine doped low K dielectric oxide gate spacer overlaps only a portion of the upper surface of the source and drain regions. The rest of the source and drain regions is contacted by the silicon nitride oxide layer described above. According to Pan, the only dielectric material that the source/drain regions contact is the fluorine doped oxide layer 18, that is, the source and drain regions of the prior art structure ***do not contact a silicon nitride oxide layer.***

As discussed above, the foregoing remarks demonstrate that Pan does not disclose each and every element of the present invention. Therefore, Pan does not teach each and every aspect of the claimed invention, as required by King and Kloster Speedsteel; therefore the currently amended Claim 16, which now positively recites the above mentioned elements of the present invention, are not anticipated by Pan. Applicants respectfully submit that the instant § 102(b) rejection has been obviated and withdrawal thereof is respectfully requested.

Concerning the 35 U.S.C. § 103(a) obviousness rejection of Claims 17 – 18 based on Pan, Applicants submit that Pan does not teach or suggest the structure of the present invention as recited in Claim 16, from which Claims 17 – 18 of the instant application depend. Applicants submit that the conductive spacer structure is necessary to enable the prior art structure. See, for example, the title of Pan which is "method of making a conductive spacer lightly doped drain (LDD) for hot carrier effect (HCE) control," implying that the conductive spacers are necessary. In contrast, the spacers according to the present invention do not contact conductive spacers, but instead a dielectric layer of silicon nitride oxide is located directly atop the low-K spacer. Since Pan requires the presence of conductive spacers, Pan does not teach or suggest the claimed structure. Applicants respectfully submit that the obviousness rejection of Claims 17 – 18 based on Pan has been obviated, and withdrawal thereof is respectfully requested.

Concerning the 35 U.S.C. § 103(a) rejection of Claims 16 – 18 based on Horstman in view of Pan, Applicants submit that Horstman cannot be combined with Pan since Horstman discloses a structure with "reduced line to line capacitance and cross talk noise" while Pan introduces an additional conducting structure (conductive spacers 22a and 22b with accompanying contacts 28b and 28d in Pan) that would increase line to line capacitance and increase cross-talk noise.

It has been well established that it is improper for the Examiner to combine references where the references *teach away* from the combination. In re Grasselli, 218 USPQ 769 (Fed. Cir. 1983). The Examiner cannot "*disregard[ing] disclosures in the references that diverge from and teach away from the invention at hand.*" Panduit Corp. v. Dennison Manufacturing Co., 227 U.S.P.Q. 337 (CAFC 1985).

Introduction of an additional metal structure can only increase capacitance of an existing structure due to the additional capacitive coupling with the new conductive structure. Furthermore, electrical signals applied to the conductor spacers of Pan only increase cross-talk noise. Since the purpose of the invention of Horstman is to reduce line to line capacitance and cross talk noise, one of ordinary skill in the arT would not attempt to combine the structure disclosed in Pan with Horstman.

Horstman alone or Pan alone do not teach or suggest the present invention. Applicants submit that Pan is defective for the reasons discussed above and, as such, the remarks made under the anticipation rejection are incorporated herein by reference. Horstman does not disclose a structure with a silicon nitride oxide layer as presently recited in amended Claim 16.

Applicants also submit that even if a combination of Horstman and Pan were to be possible (which Applicants submit it is not), the combined disclosures still do not teach or suggest a structure with a silicon nitride oxide layer as claimed in amended Claim 16 of the instant application.

Applicants respectfully submit that the 35 U.S.C. § 103(a) rejection on Claims 16 – 18 based on the combined disclosures and Horstman and Pan has been obviated, and withdrawal thereof is respectfully requested.

Concerning the 35 U.S.C. § 103(a) rejection of Claim 20 based on Horstman in view of Pan, and further in view of Kasai. As discussed above, it is improper to combine Pan with Horstman. As the Examiner acknowledged, Horstman does not disclose a silicon nitride oxide layer located on at least the gate stack, or for that matter, discussion of silicon nitride oxide cannot be found anywhere in Horstman. Therefore, there is no silicon nitride oxide layer that

contacts ***at least a portion of said source and drain regions*** and ***overlays the gate stack and the fluorine doped low K dielectric oxide gate spacers.***

Kasai discloses a structure with an insulating cap over the gate electrode as described in Column 7, line 9, "An insulating cap is formed on the gate electrode" and in Column 12, lines 1 – 3, "Two insulating caps 26 with a thickness of approximately 100 nm are formed on the two gate electrodes 25, respectively" and as is evident in FIG. 4 (first embodiment) and in FIG. 7 (second embodiment). While Kasai discloses an insulating cap layer that may be a silicon oxynitride (Column 6, lines 56 – 61), the insulating cap (elements 6A, 6B in FIG. 4 and element 26 in FIG. 7 of Kasai) is confined only to the top of the gate. The insulating cap layer does not overlay a spacer or any part of the source or drain area as can be readily seen in FIG. 4 and FIG. 7 of Kasai. Also, no motivation to extend the coverage of the insulating cap is found in Kasai since the confinement of the insulating cap within the gate region is required to enable the invention by Kasai. Therefore, one of ordinary skill in the art would not be able to combine Kasai with Horstman to enable a silicon nitride oxide layer that contacts ***at least a portion of said source and drain regions*** and ***overlays the gate stack and the fluorine doped low K dielectric oxide gate spacers.***

Applicants respectfully submit that the 35 U.S.C. § 103(a) rejection of Claim 20 based on the combined disclosures and Horstman, Pan, and Kasai has been obviated and withdrawal thereof is respectfully requested.

Concerning the 35 U.S.C. § 103(a) rejection on Claim 21 based on Kasai in view of Wasshuber and a similar rejection based on Wasshuber in view of Kasai, Applicants submit that neither of the two combinations of Kasai with Wasshuber teaches nor suggests the structure as claimed in Claim 21 of the present application.

Specifically, according to Kasai, it is required to keep the extent of the insulator cap only over the gate electrode as discussed above to enable the structure of the invention by Kasai. Extending the coverage of the cap layer, which may be a silicon oxynitride layer, according to Kasai as disclosed in Column 6, lines 56 – 61 is neither taught nor suggested in Kasai. In fact, it is required that the cap layer be confined to the gate electrode to enable Kasai's invention since extending the cap layer beyond the gate electrode would result in a different structure than what is described in Kasai.

Wasshuber discloses an oxide layer that overlays and contacts a gate stack, a cap layer which comprises "a material with a dielectric coefficient k value equal to or greater than the k value of silicon dioxide (i.e., equal to or greater than approximately 4.2)" (paragraph [0017] of Wasshuber), and remaining surfaces of the silicon substrate. Wasshuber specifically states that the cap layer has a dielectric constant has a dielectric constant "equal to or greater than the k value of silicon dioxide" where as Claim 21 of the present application specifically states "no material with a dielectric constant greater than 4.0 is present between the fluorine doped low K dielectric oxide gate spacer and the silicon nitride oxide layer." Furthermore, there is no teaching or suggestion in Wasshuber that the oxide layer 33 in Wasshuber can be replaced by an oxynitride layer. Applicants also observe the lack of any mention of deposition of a nitride over the gate stack and the spacer, or and the lack of any mention of ISSG (in-situ steam generation) process which is required to convert a nitride layer to an oxide layer in Wasshuber.

Therefore, one of ordinary skill in the art would not be able to combine the teachings of Kasai and Wasshuber to enable a structure that contains ***a silicon nitride oxide layer*** that overlays and contacts a gate stack, a fluorine doped low K dielectric oxide gate spacer, and remaining surfaces of the silicon substrate.

In other words, Wasshuber nor Kasai either alone or in combination enables a nitride oxide layer that contacts only a low K dielectric material spacer but does not contact ***a dielectric constant greater than 4.0 is present between said fluorine doped low K dielectric oxide gate spacer and said silicon nitride oxide layer***. Kasai does not provide a layer that is structurally equivalent to the nitride oxide layer of the present invention, that is, a layer that overlays and contacts a gate stack, a fluorine doped low K dielectric oxide gate spacer, and remaining surfaces of the silicon substrate. While Wasshuber may be teaching a structure that satisfied the above requirement, the structure according to Wasshuber ***contains material with a dielectric constant greater than 4.0 is present between said fluorine doped low K dielectric oxide gate spacer and said silicon nitride oxide layer***, which is a direct opposite of the structure of currently amended Claim 21.

The various § 103 rejections also fail because there is no motivation in the applied references, either individually or in practicable combinations, which suggest modifying the disclosed structures to include the various elements. Kasai does not have any structure that is equivalent the nitride oxide layer of the instant application. Wasshuber provides no motivation to form a structure ***"wherein no material with a dielectric constant greater than 4.0 is present between said fluorine doped low K dielectric oxide gate spacer and said silicon nitride oxide layer"*** as recited in currently amended Claim 21. Instead, Wasshuber teaches away from elimination of the cap layers 28 and 30 in Wasshuber by indicating that the presence of the cap layer comprising a "a dielectric coefficient k value equal to or greater than the k value of silicon dioxide" ([0017] of Wasshuber) since "Cap layers 28 and 30 have a less fragile surface than the surface of low-k spacers 20 and 22 without cap layers 28 and 30." Thus, there is no motivation provided in the applied references, or otherwise of record, to make the modification mentioned

above. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Vaeck, 947 F.2d, 488, 493, 20 USPQ 2d. 1438, 1442 (Fed.Cir. 1991).

Applicants observe that Kasai is primarily concerned with contact formation and does not utilize any layer that overlays and contacts a gate stack, a fluorine doped low K dielectric oxide gate spacer, and remaining surfaces of the silicon substrate. Applicants also observe that the presence of cap layers with a dielectric coefficient k value equal to or greater than the k value of silicon dioxide is essential for the invention disclosed in Wasshuber. Applicants submit that combination of these two prior art references does not enable the invention as claimed in Claim 21 of the instant application.

Applicants respectfully submit that the 35 U.S.C. § 103(a) rejections on Claim 21 based on the combined disclosures and Horstman and Kasai have been obviated and withdrawal thereof is respectfully requested.

Wherefore, reconsideration and allowance of the claims in the currently amended form of the present application are respectfully requested.

Also, in view of the foregoing amendments and remarks, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited

Respectfully submitted,

Leslie S. Szivos, Ph.D.
Registration No. 39,394

Scully, Scott, Murphy & Presser, P.C.
400 Garden City Plaza, Suite 300
Garden City, New York 11530
(516) 742-4343 (phone)
(516) 742-4366 (facsimile)

Customer No.: 23389

LSS/BP/tam